REMARKS

This paper is responsive to the Final Office Action dated March 17, 2005. Claims 1-56 were examined.

Information Disclosure Statement

The Examiner's attention is directed to an Information Disclosure Statement (IDS) filed on March 16, 2005. Consideration of this IDS is requested, with initialed listings of the references considered included in the next Office action.

Claim Rejections - 35 U.S.C. § 112

Claims 25 and 27 stand as rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 25 has been canceled.

Regarding claim 27, the Examiner has questioned how the claimed limitations relate to claim 1. Claim 27, as amended, adds to claim 1 the limitation that each of the first Y-line group is configured to be simultaneously selected in a read mode of operation, and each of the second Y-line group is configured to be simultaneously selected in a read mode of operation. Examples of a structure illustrating this limitation include that shown in Fig. 6 (the first Y-line group including BL1-BL4 and the second Y-line group including BL5-BL8), and also that shown in Fig. 7, Fig. 8, Fig. 9, and Fig. 11. Applicant respectfully requests this rejection be withdrawn.

Claim Rejections - 35 U.S.C. § 103

Claims 1-5, 8, 9, 13-24, 26, 28-33, 37-43, 46-53 and 56 stand as rejected under 35 U.S.C. § 103(a) as being unpatentable over Kobayashi, et al. (U. S. Patent No. 5,337,281) in view of Kato, et al. (U. S. Patent No. 6,741,509). Applicant has amended certain of the claims, and believes this rejection has been overcome.

Applicant has amended claim 1 to now recite:

> A non-volatile memory cell array comprising within a first array block a first plurality of X-lines configured to be simultaneously selected ~~logically identical~~ in a read mode of operation, and each associated with a first Y-line group numbering at least one Y-line.

This amendment makes clear that the first plurality of X-lines are all found within a first array block. As this claim was originally filed, such a limitation was intended by the definition of "array" provided at page 19, paragraph 1066, at lines 3-6. Nonetheless, the Examiner has given the language of originally-filed claim 1 (e.g., "A non-volatile memory cell array") a broader meaning than intended by the originally-filed definition of array. Consequently, the limitation of "within a first array block" has been added, which is consistent with the teachings of the disclosure, and also not inconsistent with common usage in the art of "array block" (also sometimes referred to as a "sub-array" or "memory block"). The amended claim 1 also now recites that the first plurality of X-lines are configured to be simultaneously selected (rather than logically identical). This amendment is not believed to be a narrowing amendment, and is believed to overcome the rejection of claim 1.

Kato discloses a memory array in which more than one word line may be simultaneously activated, but such word lines may be located within different memory blocks. The number of word lines which can be used to simultaneously read/write independent data items in the memory cell array is determined by the data line configuration in the memory cell array. For example, in certain embodiments, a total of 16 Master DQ line pairs (MDQP) are used to access data within the memory cell array, which are each coupled to a respective one-fourth of the memory array (i.e., in Fig. 59, MDQPa<0:3> coupled to sense amplifier banks within region "a", MDQPb<0:3> coupled to sense amplifier banks within region "b", etc.) (See column 43, line 50 through column 44, line 21) The total number of word lines used to simultaneously read/write independent data is thus four. Applicant submits that such simultaneously activated word lines are each associated with a different memory block (i.e., array block), and thus different bit line groups.

Kato also discloses certain embodiments including sequentially accessing more than one word line, in which once-activated word lines are held in the activated state during a plurality of successive word line selection cycles. For example, in Figs. 5-12 Kato discloses a memory cell

array having a stacked-word-line test mode (i.e., a "Multiple WL test Mode") in which more than one word line is simultaneously activated, and in which

> the number of word lines which can be activated for some bit line pairs and sense amplifiers associated therewith (which are collective referred to as a memory block) is only one. Further, when the sense amplifiers are commonly used or shared by adjacent memory blocks (shared sense amplifier), the word line can be selected in only either of the memory blocks which commonly use the sense amplifiers. In other words, a maximum of N/2 word lines can be selected in a memory cell array having N memory blocks. (Column 11, lines 44-56)

None of these simultaneously selected word lines are associated with the same memory block.

Kato also discloses certain embodiments including a stacked-word-line *test mode* in which more than one word line is simultaneously activated within the *same* memory block. However, such embodiments are subject to the limitation that the contents of memory cells connected to a plurality of word lines selected in the memory block must be the same on the identical column. Otherwise data destruction will occur. (Column 27, lines 54-65)

As described, the first word line in the block is activated and the sense amplifiers activated to sense and latch data on the bit lines. Then, in the second cycle, the sense amplifier is already activated before the second word line is driven active. The sense operation of the bit line is terminated and the state is held. The same data as those of the memory cells connected to the first selected word line are *written* into second selected word line in the same memory block when the second word line is selected and the word line potential rises. (column 31, line 62 through column 32, line 5) The second word line to be selected in a memory block cannot be read, but only written with the data previously read from the first selected word line. Such operation cannot be viewed as consistent with simultaneously selecting two word lines in a *read mode* of operation.

In the first passage cited by the Examiner (column 43, lines 36-49), the embodiment described specifically requires that the four simultaneously activated word lines cannot be activated in the identical memory block nor in adjacent memory blocks (if using shared sense amplifiers) in order to prevent occurrence of data destruction (lines 44-49). Each of these word

lines is associated with a different memory block. Moreover, each of these word lines is also associated with a different bit line group.

In the second passage cited by the Examiner (column 47, lines 55-65), the embodiment described specifically states that independent data items can be simultaneously read/written with respect to four total word lines, one selected from each of regions "a", "b", "c", and "d" in Fig. 59 (lines 60-62). Each of these word lines is associated with a different memory block, and thus different bit line groups.

In the third passage cited by the Examiner (column 61, lines 35-39), the cited text describes

> word lines which are activated together in the memory cell array and used for reading/writing independent data simultaneously based on the data line configuration are set to read/write independent data items are set to belong to the same repair region. [sic]

Such a structure is described above, and refers to the data line structures (e.g., the MDQP lines) and their organization with respect to the memory cell array. Such simultaneously activated word lines are not within the same memory block, as described above. Each of these word lines is associated with a unique row address. Moreover, each is associated with a different memory block, and thus different bit line groups.

The Examiner most recently has cited Kato at column 43, lines 36-38 and 50-53 for its alleged teaching of word lines that are simultaneously activated in the cell array unit for read/write operation. Applicant respectfully notes that Kato's "cell array unit" includes many memory "blocks" (see column 11, lines 55-56), and thus teaches activating only one word line per memory block. This passage of Kato actually teaches away from the claimed invention (see column 43, lines 44-49, which states "Further, the simultaneously activated four word lines cannot be activated in the identical memory block in order to prevent occurrence of data destruction and they cannot be activated in the adjacent blocks in which the bit line pairs in the memory blocks commonly utilize the sense amplifier.").

Regarding the other independent claims 29, 38 and 51, Applicant has amended these claims similarly. For example, claim 29 has been amended to now recite (in part):

> programming individual memory cells associated with a first X-line group of at least one X-line within a first array block and further associated with a first Y-line group of at least one Y-line within the first array block until a desired first aggregate memory cell read current is obtained when simultaneously selecting all the first group of X-lines and all the first group of Y-lines, at least one of the first X-line group and first Y-line group including more than one such X-line or Y-line;

Such amendment makes clear that the first X-line group and the first Y-line group are both disposed within the same array block. In addition, the claim now explicitly requires at least one of the X-line group and the Y-line group to have more than one such X-line or Y-line.

Independent claims 38 and 51 have been amended analogously. As a result, this rejection is believed to have been overcome.

Claims 1-5, 8-24, 26, 28-56 stand as rejected under 35 U.S.C. § 103(a) as being unpatentable over Scheuerlein, et al. (U. S. Publication No. 2004-0100852) in view of Kato, et al. (U. S. Patent No. 6,741,509). The Examiner has again relied upon Kato for allegedly providing the same teaching as described above, and has presented the same argument, citing the same three passages, with the same conclusion. Applicant's amendment of the claims is believed to overcome this rejection for the same reasons as described above.

Claims 1-10, 12, 14-24, 26, 28-34, 36, 38-44 and 47-54 stand as rejected under 35 U.S.C. § 103(a) as being unpatentable over Iwata, et al. (U. S. Publication No. 2003-0161197) in view of Kato, et al. (U. S. Patent No. 6,741,509). The Examiner has again relied upon Kato for allegedly providing the same teaching as described above, and has presented the same argument, citing the same three passages, with the same conclusion. Applicant's amendment of the claims is believed to overcome this rejection for the same reasons as described above.

Applicant submits that, at best, the cited references (particularly Kato) disclose activating during a read mode a single word line in each of several memory array blocks, and in a certain test mode, activating more than one word line in a memory array block. Such a test mode is

described as useful for voltage stressing a memory array (e.g., Kato, at column 53, lines 1-7), cannot be used in a read mode if more than one word line per array block is activated, and when used the identical data must be previously written into memory cells associated with each word line.

There is nothing in the teaching of Kato, combined with either of Kobayashi, Scheuerlein, or Iwata to suggest a non-volatile memory cell array comprising a first plurality of X-lines configured to be simultaneously selected in a read mode of operation, and each associated with a first Y-line group numbering at least one Y-line, as recited in Applicant's claim 1. Even assuming, *arguendo*, that these references are so combined, the teaching of these four references still does not arrive at the claimed limitation. Consequently, Applicant respectfully requests the rejections be withdrawn.

Consistent with the arguments presented elsewhere herein, Applicant's use of "simultaneously selecting" more than one array line (e.g., X-line; Y-line, etc.) does not necessarily require such lines be driven to the selected state and/or returned to the unselected state (i.e., activated and/or inactivated, selected and/or unselected) at precisely the same times, but only requires that at some time each of the group of such simultaneously selected lines are all in fact selected.

Other Amendments

Claim 3 has been amended to replace an upper-case "L" character with a lower-case character.

Claims 8, 9, 19, 20, 21, and 27 have been amended consistent with the amendments to claim 1.

Claims 17 and 49 have been amended to more clearly indicate that the first plurality of X-lines are disposed on only a single layer of the memory array.

Claims 20 and 21 have been further amended to clarify when the two recited pluralities of X-lines (in each respective claim) are each simultaneously selected.

Claim 43 has been amended to clarify that the third X-line group is not necessarily selected at all times "whenever" the first X-line group is not selected.

Claim 48 has been amended to add an omitted word, and now recites "on more than one layer of the memory array".

Summary

Claims 1-24 and 26-56 are in the case. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited.

Should any issues remain, Applicant respectfully requests a telephonic interview with the Examiner to discuss this response, and further in the hope that the remaining issues might be efficiently resolved.

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Andrew C. Graham — 5-17-05 Date

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